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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,827	05/26/2006	Masanori Dainin	R2184.0501/P501	7587

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,827	DAININ, MASANORI	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on May 26, 2006. Claims 1-12 are pending.

Claim Objection

1. ** Claim 6 is objected to since "said polysilicon" at line 6 should be -- said polysilicon pattern -- so as to provide proper antecedent basis.

** Claim 11 is objected to since "the metal interconnection layer " at last line should be – the metal interconnection layer pattern -- so as to provide proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1,2,4,11, and 12 are rejected under 35 U.S.C. 102(a)/(e) as being anticipated by Nakatani et al (2005/0051899).

Re claim 1, Nakatani teaches a semiconductor device and method thereof comprising: a semiconductor substrate 11; a polysilicon pattern 15 (Fig 2a-2g,3; paragraphs 43-58; Figs 1, paragraphs 35-42) formed on said semiconductor substrate via an insulation film 12; an interlayer insulation film 13 (paragraphs 43-44) formed on said semiconductor substrate so as to cover said polysilicon pattern 15; and a metal interconnection layer pattern 19/20 (paragraphs 49-50) formed on said interlayer insulation film 16U/13, wherein said metal interconnection layer pattern carrying silicon nitride films 25,16S (Fig 3; paragraphs 54-56, 37,47) respectively

on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3). Re claim 2, wherein said silicon nitride films comprises a first nitride film 16S formed on a surface of said interlayer insulation film 16U and in contact with a bottom surface of said metal interconnection layer pattern 19/20, and a second nitride film 25 covering said sidewall surfaces and top surface of said metal interconnection layer pattern 19/20 (Fig 3; paragraphs 54-55, 37,47; Figs 2a-2g, paragraphs 43-58). Re claim 4, wherein there is provided a region where said first nitride film 16S and said second nitride film 25 are removed to provide openings for external connections, except for said first nitride film 16S underlying said metal interconnection layer pattern 19/20 (Fig 3, paragraphs 54-56,52; Fig 2e, paragraph 47). Re claim 11, Nakatani teaches a semiconductor device and method thereof comprising: forming a polysilicon pattern 15 on a semiconductor substrate 11 via an insulation film 12 (Fig 2a-2g,3; paragraphs 43-58; Figs 1, paragraphs 35-42); forming an interlayer insulation film 16U/13 (paragraphs 43-44) on said semiconductor substrate so as to cover said polysilicon pattern 15; forming a first nitride film 16S on the interlayer insulation film 16U/13; forming a metal interconnection layer pattern 19/20 (paragraphs 49-50) on the first nitride film 16S formed on said interlayer insulation film 16U/13; and forming a second nitride film 25 on the first nitride film 16S so as to cover the metal interconnection layer pattern 19/20 (Fig 3; paragraphs 54-56, 37,47) respectively on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3). Re claim 12, further comprising the step, after said step of forming said second nitride film 25, of removing said second nitride film 25 and said first nitride film selectively from a predetermined area (Fig 3, paragraphs 54-56,52; Fig 2e, paragraph 47) in order to provide openings for external connections.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 102(a)/(e) as being anticipated by Nakatani et al (2005/0051899) taken with Oku (5,812,364).

Nakatani teaches a semiconductor device as applied in claim 1 above and fully repeated herein, wherein said metal interconnection layer pattern 19/20 (paragraphs 49-50) carrying silicon nitride films including the first silicon nitride 16S and a second silicon nitride 25 (Fig 3; paragraphs 54-56, 37,47) respectively on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3).

Nakatani does not mention the first nitride film and said second nitride film having different thicknesses.

However, Oku teaches (at Fig 1) the first nitride film and said second nitride film having different thicknesses, wherein the first silicon nitride film 5 of 500 Angstroms (col 5, lines 13-22) is having thickness different from the second silicon nitride film 9 of about 5000 Angstroms in thickness (col 5, lines 30-40).

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to form the semiconductor device of Nakatani by selecting the portion of the prior art's range of thickness for the first silicon nitride film and the second silicon nitride film, wherein the first silicon nitride film is having thickness different from the second silicon nitride film, as taught by Oku, which thickness is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

6. Claims 1,2,4-7,11,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (EP-1310998-A2) taken with Nakatani et al (2005/0051899).

Re claim 1, Shimizu teaches a semiconductor device comprising a semiconductor substrate 1 (Figs 2 3A-3C,12, paragraphs 62-98), a polysilicon pattern 37 (e.g. paragraphs 71-78; Figs 2,3A-3C,1) formed on a semiconductor substrate via an insulation film 9, an interlayer

insulation film 45/49 (paragraphs 74-78) being formed on said semiconductor substrate so as to cover said polysilicon pattern 37, a metal interconnection layer pattern 47/51 (Figs 2,3A,3C,1; paragraphs 75-78) being formed on said interlayer insulation film, wherein a second silicon nitride film 53 (SiN) covers the top surface and side surfaces of the metal interconnection layer pattern 51 (Fig 2, paragraph 78). Re claim 11, Shimizu teaches a method of fabricating a semiconductor device comprising, forming a polysilicon pattern 37 (e.g. paragraphs 71-78; Figs 2,3A-3C,1) on a semiconductor substrate 1 (Figs 2 3A-3C,12, paragraphs 62-98)via an insulation film 9; forming an interlayer insulation film 45/49 (paragraphs 74-78) on said semiconductor substrate so as to cover said polysilicon pattern 37; forming a metal interconnection layer pattern 47/51 (Figs 2,3A,3C,1; paragraphs 75-78) being formed on said interlayer insulation film. Re claim 4, wherein portions of the upper insulating films 49,53 are removed to form openings therein so as external connections can be formed. Re claim 5, wherein said semiconductor device further comprises a p-channel MOS transistor having a gate electrode 13 formed of said polysilicon pattern, formation of said metal interconnection layer pattern, wherein a third silicon nitride film 41 is formed in a region over said p-channel MOS transistor (Figs 2; paragraphs 2,63-73). Re claim 6, wherein there is provided a laminated film between said polysilicon pattern 37 and said interlayer insulation film 45 (Fig 2), said laminated film comprising consecutive lamination of an oxide film 39 and a third nitride film 41 in a direction from said polysilicon pattern 37 to said interlayer insulation film 45 (Fig 2, paragraphs 71-74). Re claim 7, wherein said semiconductor device further comprises a p-channel MOS transistor having a gate electrode 13 of said polysilicon pattern 37, said third nitride film 41 being formed over said p-channel MOS transistor (Figs 1-2; paragraphs 71-74,20-21,18). Re claim

Shimizu lacks forming the first silicon nitride and a second silicon nitride film so as the metal interconnection layer pattern carrying silicon nitride films respectively on a top surface, a bottom surface and sidewall surfaces thereof (Base claims 1,11 with dependent claims 2,4,12).

However, Nakatani teaches forming a first silicon nitride film 16S on the interlayer insulation film 16U/13 formed over a polysilicon pattern 15 (Fig 2a-2g,3; paragraphs 43-58; Figs 1, paragraphs 35-42); and forming a second nitride film 25 on the metal interconnection layer pattern 19/20 (Fig 3; paragraphs 54-56, 37,47) so that the metal interconnection layer

pattern 19/20 carrying silicon nitride films 25,16S (Fig 3; paragraphs 54-56, 37,47) respectively on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3); wherein said silicon nitride films comprises a first nitride film 16S formed on a surface of said interlayer insulation film 16U and in contact with a bottom surface of said metal interconnection layer pattern 19/20, and a second nitride film 25 covering said sidewall surfaces and top surface of said metal interconnection layer pattern 19/20 (Fig 3; paragraphs 54-55, 37,47; Figs 2a-2g, paragraphs 43-58, re further claim 2); wherein there is provided a region where said first nitride film 16S and said second nitride film 25 are selectively removed to provide openings for external connections from a predetermined area, except for said first nitride film 16S underlying said metal interconnection layer pattern 19/20 (Fig 3, paragraphs 54-56,52; Fig 2e, paragraph 47, re further claims 4,12).

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the semiconductor device of Shimizu by forming the first silicon nitride film on the interlayer insulation film and forming the second nitride film on the metal interconnection layer pattern, and opening therein for external connections, as taught by Nakatani. This is because of the desirability to passivate and protect the metal interconnect layer pattern with the barrier silicon nitride films having an excellent in corrosion resistance, thereby improve the reliability of the semiconductor device, wherein external connections to the metal interconnection layer pattern can be formed by selectively removing a portion of the silicon nitride films from a predetermined area.

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (EP-1310998-A2) taken with Nakatani et al (2005/0051899), as applied to claims 1,2,4-7,11-12 above, and further of Itoh (2002/0180453).

The references of Shimizu and Nakatani teach a semiconductor device as applied to claims 1,2,4-7,11 and 12 above, and fully applied and repeated herein for claims 8,9 and 10, in which Nakatani also teaches a semiconductor device and method thereof comprising: a semiconductor substrate 11; a polysilicon pattern 15 (Fig 2a-2g,3; paragraphs 43-58; Figs 1, paragraphs 35-42) formed on said semiconductor substrate via an insulation film 12; an interlayer insulation film 13 (paragraphs 43-44) formed on said semiconductor substrate so as to

cover said polysilicon pattern 15; and a metal interconnection layer pattern 19/20 (paragraphs 49-50) formed on said interlayer insulation film 16U/13, wherein said metal interconnection layer pattern carrying silicon nitride films 25,16S (Fig 3; paragraphs 54-56, 37,47) respectively on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3). Re further claim 8, Shimizu also already teaches the semiconductor device having a voltage divider circuit producing an output voltage by dividing a voltage supplied thereto, said voltage divider circuit comprising two or more resistance elements R1 and R2 (Figs 13-14,12, paragraphs 133,136-140; col 13, paragraphs 58-60; paragraphs 131-133,136-140), said resistance element comprising a polysilicon pattern 37 (e.g. paragraph 71; Figs 1,2-3C). Re further claim 9, Shimizu also already teaches a semiconductor device comprising a voltage divider circuit dividing a voltage supplied thereto and producing an output voltage (Figs 1,2,12,13,14; col 13, paragraphs 58-60; paragraphs 131-133,136-140); a reference voltage generator (paragraph 58-59) supplying a reference voltage; and a comparator circuit (paragraph 59) comparing said output voltage of said voltage divider circuit with said reference voltage of said reference voltage generator, said voltage divider circuit comprising two or more resistance elements R1 and R2 (Figs 13-14,12, paragraphs 133,136-140; col 13, paragraphs 58-60; paragraphs 131-133,136-140), said resistance element comprising a polysilicon pattern 37 (e.g. paragraph 71; Figs 1,2-3C). Re further claim 10, Shimizu also already teaches a semiconductor device comprising an output driver controlling an output of an input voltage (Figs 13-14,12; paragraphs 132,131,133-139); a voltage divider circuit dividing a voltage supplied thereto and producing an output voltage (Figs 1,2,12,13,14; col 13, paragraphs 58-60; paragraphs 131-133,136-140); a reference voltage generator (paragraph 58-59) supplying a reference voltage; and a constant voltage generator having a comparator circuit comparing said divided voltage from said voltage divider circuit and said reference voltage from said reference voltage generator, said comparator circuit controlling said output driver in response to a result of comparison, said voltage divider circuit comprising two or more resistance elements R1 and R2 (Figs 13-14,12, paragraphs 133,136-140; col 13, paragraphs 58-60; paragraphs 131-133,136-140), said resistance element comprising a polysilicon pattern 37 (e.g. paragraph 71; Figs 1,2-3C)

Re claims 8, 9,10, Shimizu thus lacks having the output voltage of the voltage divider being adjustable by disconnection of a fuse element.

However, Itoh teaches (at Figs 1-7; paragraphs 4-16; 74-92) a semiconductor device, in which the output voltage of the voltage divider (Fig 5, paragraphs 83-97) is being adjustable by disconnection of a fuse element (e.g. Figs 1,2, RLO-RL3), paragraphs 74+).

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor of the relied references of Shimizu and Nakatani by having the output voltage of the voltage divider being adjustable by disconnection of a fuse element, as taught by Itoh. This is because of the desirability to adjust the resistance of the resistance elements and to provide an error correction to the semiconductor device, thereby improving the reliability of the semiconductor device.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (EP-1310998-A2) taken with Nakatani et al (2005/0051899), as applied to claims 1,2,4-7,11,12, and further of

The references of Shimizu and Nakatani teach a semiconductor device as applied to claim 1 above and fully repeated herein, in which Nakatani teaches the metal interconnection layer pattern 19/20 (paragraphs 49-50) carrying silicon nitride films including the first silicon nitride 16S and a second silicon nitride 25 (Fig 3; paragraphs 54-56, 37,47) respectively on a top surface, a bottom surface and sidewall surfaces thereof (Fig 3).

The references do not mention the first nitride film and said second nitride film having different thicknesses.

However, Oku teaches (at Fig 1) the first nitride film and said second nitride film having different thicknesses, wherein the first silicon nitride film 5 of 500 Angstroms (col 5, lines 13-22) is having thickness different from the second silicon nitride film 9 of about 5000 Angstroms in thickness (col 5, lines 30-40).

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to form the semiconductor device of the references by selecting the portion of the prior art's range of thickness for the first silicon nitride film and the second silicon nitride film, wherein the first silicon nitride film is having thickness different from the second silicon nitride film, as taught by Oku, which thickness is within the range of applicant's claims, because it has been held to be obvious to select a value in a known

range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-24-4

/Michael Trinh/
Primary Examiner, Art Unit 2822